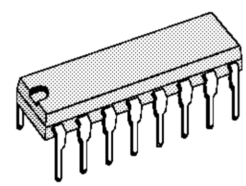
SGS-THOMSON MICROELECTRONICS

# TDA1180P

## TV HORIZONTAL PROCESSOR

- NOISE GATED HORIZONTAL SYNC SEPARATOR
- NOISE GATED VERTICAL SYNC SEPARATOR
- HORIZONTAL OSCILLATOR WITH FREQUENCY RANGE LIMITER
- PHASE COMPARATOR BETWEEN SYNC PULSES AND OSCILLATOR PULSES (PLL)
- PHASE COMPARATOR BETWEEN FLYBACK PULSES AND OSCILLATOR PULSES (PLL)
- LOOP GAIN AND TIME CONSTANT SWITCHING ( VCR)
- COMPOSITE BLANKING AND KEY PULSE GENERATOR
- PROTECTION CIRCUITS
- OUTPUT STAGES WITH HIGH CURRENT CAPABILITY



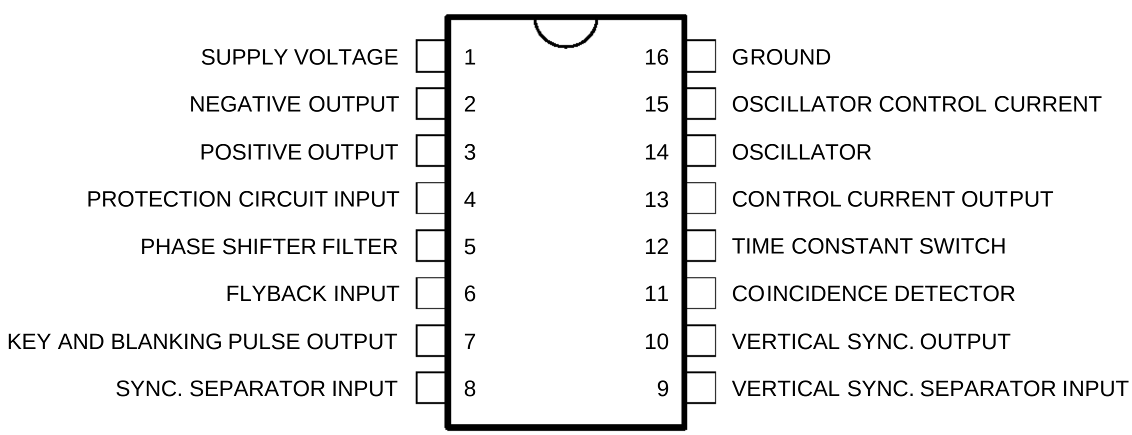
**DIP16**
(Plastic Package)

**ORDER CODE :** TDA1180P

### DESCRIPTION

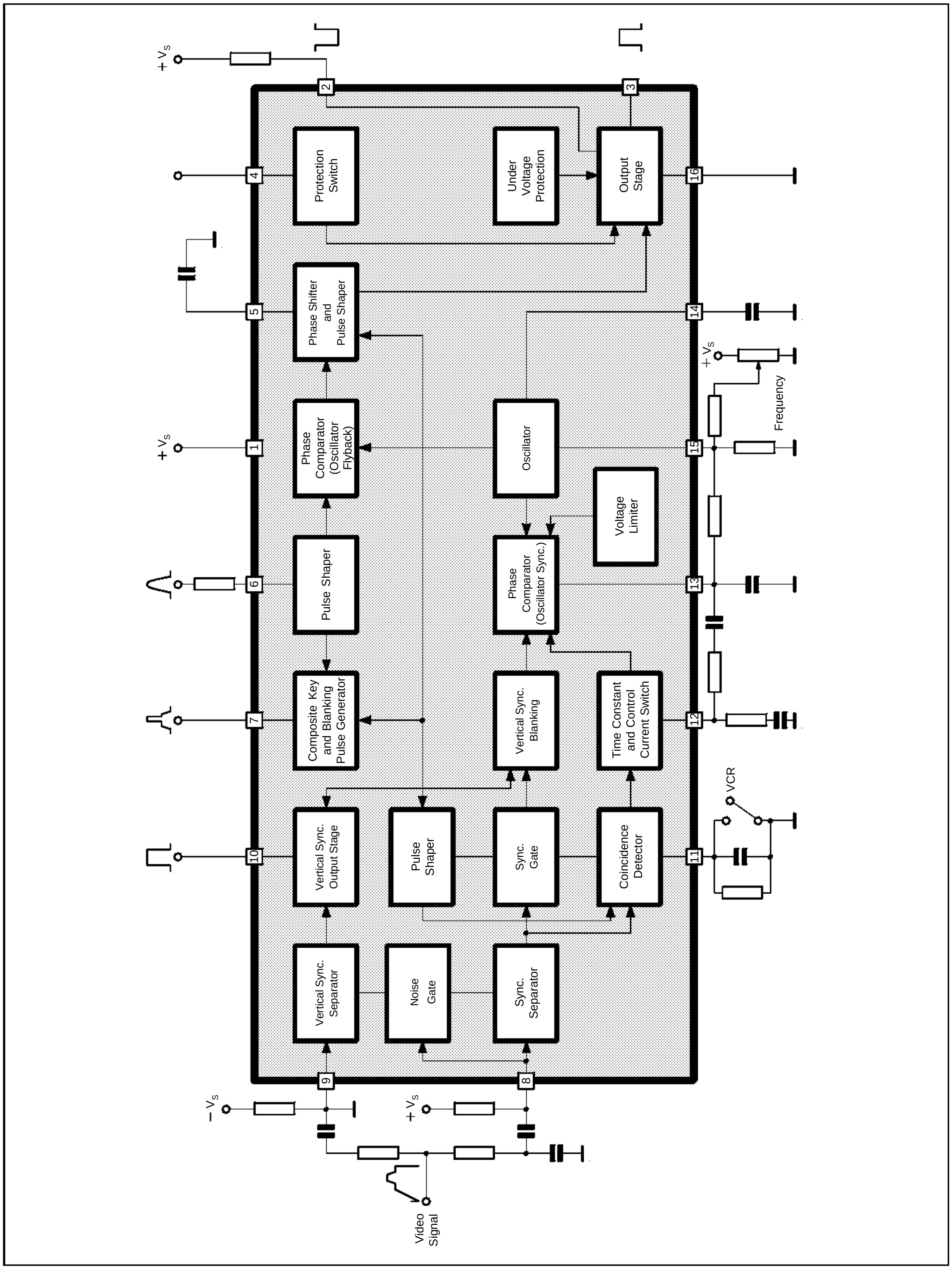
The TDA1180P is a horizontal processor circuit for b.w. and colour monitors. It is a monolithic integrated circuit encapsulated in 16-lead dual in-line plastic package.

### PIN CONNECTIONS




1180P-01.EPS

## BLOCK DIAGRAM




1180P-02.EPS



SGS-THOMSON MICROELECTRONICS

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_S$ | Supply voltage (Pin 1) | 15 | V |
| $V_2$ | Voltage at Pin 2 | 18 | V |
| $V_4$ | Voltage at Pin 4 | $V_S$ | |
| $V_8$ | Voltage at Pin 8 | - 6 , $V_S$ | V |
| $V_9$ | Voltage at Pin 9 | ± 6 | V |
| $V_{11}$ | Voltage at Pin 11 | $V_S$ | |
| $I_2$ | Pin 2 peak current | 1 | A |
| $I_3$ | Pin 3 peak current | 0.5 | A |
| $I_6$ | Pin 6 current | 30 | mA |
| $I_7$ | Pin 7 current | 20 | mA |
| $I_{10}$ | Pin 10 current | 30 | mA |
| $P_{tot}$ | Total power dissipation at Tamb ≤ 70°C | 1 | W |
| $T_{stg}$ , $T_j$ | Storage and junction temperature | - 40 , + 150 | °C |

1180P-01.TBL

## THERMAL DATA

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $R_{th\ (j-a)}$ | Thermal Resistance Junction-Ambient | Max | 80 | °C/W |

1180P-02.TBL

## ELECTRICAL CHARACTERISTICS

(refer to the test circuit, $V_S$ = 12V, $T_A$ = 25°C, unless otherwise specified)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_S$ | Supply voltage range | | 9.5 | 12 | 13.2 | V |
| $I_S$ | Supply current | $I_3$ = 0 | | 42 | 52 | mA |
| $V_S$ | Supply voltage at which the output pulses (at pin 2 and 3) are switched off | | | | 4 | V |
| HORIZONTAL SYNC. SEPARATOR | | | | | | |
| $V_I$ | Peak to peak input signal | | 1 | 3 | 6 | V |
| $V_8$ | Input switching voltage | $I_8$ = 80 µA | | 1.5 | | V |
| $I_8$ | Input switching current | $V_8$ = 1.4V | | 10 | | µA |
| $I_8$ | Leakage current | $V_8$ = -5V | | | 1 | µA |
| VERTICAL SYNC. SEPARATOR | | | | | | |
| $V_I$ | Peak to Peak Input Signal | | 1 | 3 | 6 | V |
| $V_9$ | Input Switching Voltage | $I_9$= 80µA | | 1.5 | | V |
| $I_9$ | Input Switching Current | $V_9$ = 1.4V | | 5 | | µA |
| $I_9$ | Leakage Current | $V_9$ = -5V | | | 1 | µA |
| $V_{10}$ | Vertical Sync. Pulse Output Voltage | No Load Pin10 | 11 | | | V |
| $R_{10}$ | Output Resistance | | | 10 | | kΩ |
| $t_{LV}$ | Delay between Leading Edge of Input and Output Signals | | | 17 | | µs |
| $t_{LV}$ | Delay between Trailing Edge of Input and Output Signals | | | 50 | | µs |
| $t_V$ | Vertical Sync Pulse Duration | | | 190 | | µs |

1180P-03.TBL

## ELECTRICAL CHARACTERISTICS (continued)

(refer to the test circuit, $V_S$ = 12V, $T_A$ = 25°C, unless otherwise specified)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| PROTECTION CIRCUIT | | | | | | |
| $V_4$ | Input Voltage for Switching off the Output Pulses | Output Pulses OFF<br>Output Pulses ON | <br>1 | | 0.5 | V |
| $R_4$ | Input Resistance | | | 200 | | kΩ |
| $I_4$ | Input Current | | 5 | | | µA |
| FLYBACK PULSE | | | | | | |
| $V_6$ | Input Threshold Voltage of Blanking Generator | | | 1.8 | | V |
| $V_6$ | Input Threshold Voltage of Phase Comparator | | | 7.6 | | V |
| $I_6$ | Input Switching Current | $V_6 \geq$ 1.7V | | 0.45 | | mA |
| OUTPUT PULSE | | | | | | |
| $V_3$ | Peak-to-Peak Output Voltage | $I_3$ = 150 mApp | | 10 | | V |
| $I_3$ | Output Current | $V_3$ = 5V | | 500 | | mA |
| $R_3$ | Output Resistance | At Leading Edge of output pulse<br>At Training Edge of Output Pulse | | 3<br>20 | | Ω<br>Ω |
| $t_p$ | Output Pulse Duration | | 20 | 22 | 26 | µs |
| COMPOSITE BLANKING AND KEY PULSE | | | | | | |
| $V_{7k}$ | Key Pulse Output Peak Voltage | | 9 | 11 | | V |
| $V_{7B}$ | Blanking Pulse Output Voltage | | 4.2 | 4.5 | 4.8 | V |
| $R_7$ | Output Resistance | | | 100 | | Ω |
| $t_{sk}$ | Phase Relation Between Trailing Edge of Key Pulse and Middle of Sync. Input Pulse | | | 2.7 | | µs |
| $t_k$ | Key Pulse Duration | | 3.5 | 3.8 | | µs |
| $t_{fb}$ | Delay between Flyback Pulse and Blanking Pulse | $V_6$ = 1.7V | | | 0.2 | µs |
| INTERNAL GATING PULSE | | | | | | |
| $t_g$ | Gating Pulse Duration | | | 7.5 | | µs |
| t | Phase Relation between Middle of Sync. Pulse and Trailing and Leading Edge of Gating Pulse | | | 3.75 | | µs |
| COINCIDENCE DETECTOR | | | | | | |
| $V_{11}$ | Output Voltage | With Coincidence<br>Without Coincidence | | 6.8 | <br>4 | V<br>V |
| $I_{11}$ | Peak Output Current | | | 0.5 | | mA |
| VCR SWITCH | | | | | | |
| $V_{11}$ | Input Voltage | | 0 to 4 or 8.5 to 12 | | | V |
| $-I_{11}$ | Output Current | | 35 | | | µA |
| $I_{11}$ | Output Current | | 0.4 | | | mA |
| TIME CONSTANT SWITCH | | | | | | |
| $V_{12}$ | Output Voltage | | | 3 | | V |
| $R_{12}$ | Output Resistance | 4.5V < $V_{11}$ < 8V<br>$V_{11}$ > 8.5V or $V_{11}$ < 4V | | 100<br>40 | | Ω<br>kΩ |

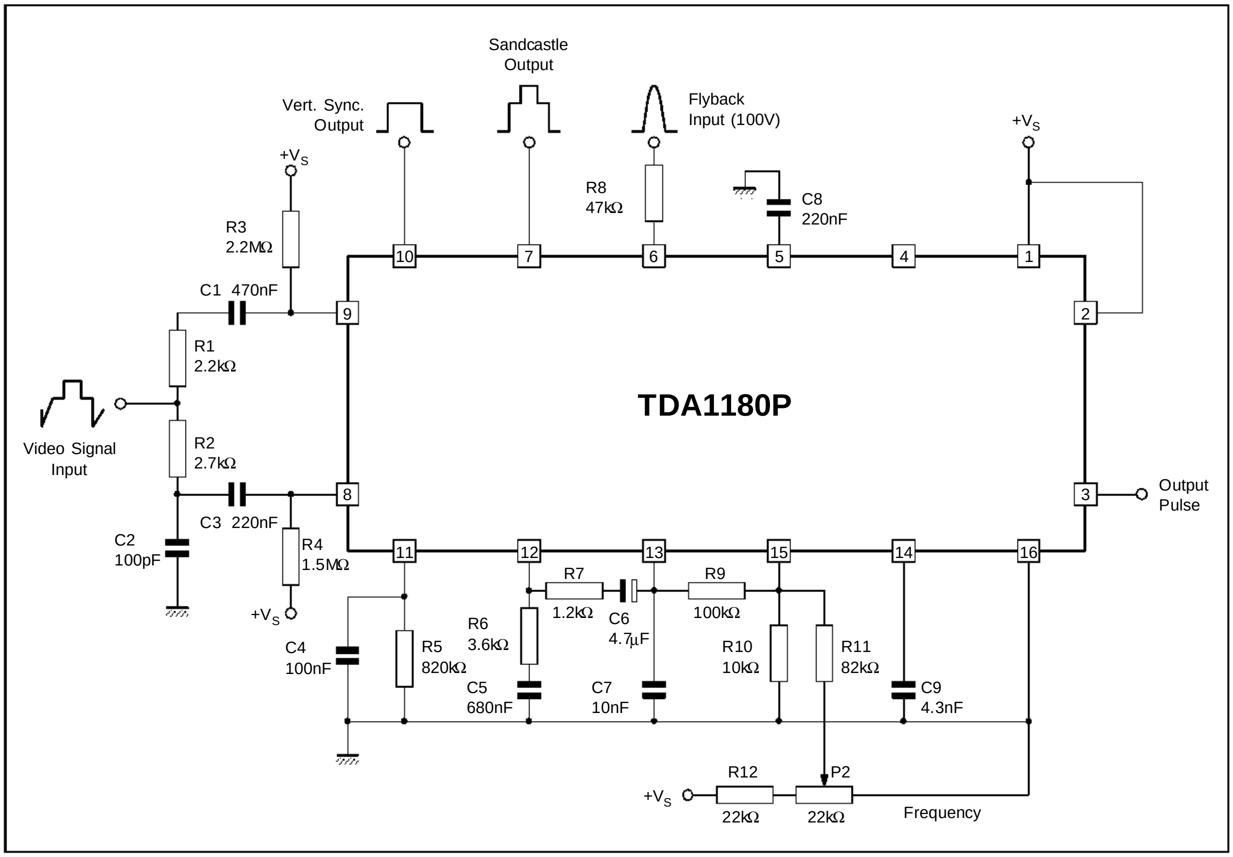
1180P-04.TBL

**ELECTRICAL CHARACTERISTICS** (continued)
(refer to the test circuit, $V_S$ = 12V, $T_A$ = 25°C, unless otherwise specified)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **OSCILLATOR** | | | | | | |
| $V_{14}$ | Low Level Threshold Voltage | | | 5.4 | | V |
| $V_{14}$ | High Level Threshold Voltage | | | 8.2 | | V |
| $I_{14}$ | Charge Current | | | 0.6 | | mA |
| $I_{14}$ | Discharge Current | | | 0.3 | | mA |
| $V_{15}$ | Current Source Supply Voltage | | | 3 | | V |
| $I_{15}$ | Current Source Supply Current | | | 0.3 | | mA |
| $f_O$ | Free Running Frequency | | | 15625 | | Hz |
| $\frac{\Delta f_O}{f_O}$ | Adjustment Range | | | ± 10 | | % |
| $\frac{\Delta f_O}{\Delta I_{15}}$ | Frequency Control Sensitivity | | | 52 | | $\frac{Hz}{\mu A}$ |
| $\Delta f_O$ | Frequency Change when $V_S$ Drops to 4V | | | | ± 10 | % |
| **OSCILLATOR-FLYBACK PULSE PHASE COMPARATOR** | | | | | | |
| $V_5$ | Control Voltage Range | | 9.4 to 8.2 | | | V |
| $I_5$ | Peak Control Current | | -0.6 | | +0.6 | mA |
| $I_5$ | Input Current (blocked Phase Detector) | | | | 5 | μA |
| $t_D$ | Permissible Delay between Output Pulse Leading Edge and Flyback Pulse Leading Edge | | | $t_p - t_f$ | | μs |
| $\frac{\Delta t}{\Delta t_D}$ | Static Control Error | | | | 0.2 | % |
| **SYNC PULSE-OSCILLATOR PHASE COMPARATOR** | | | | | | |
| $V_{13}$ | Control Voltage Range | | 4.6 to 1.4 | | | V |
| $I_{13}$ | Control Peak Current | | +2 | -2.2 | -2 | mA |
| $\frac{\Delta f}{\Delta t}$ | Phase Lock Loop Gain | | | 2 | | $\frac{kHz}{\mu s}$ |
| f | Catching and Holding Range | | | ± 700 | | Hz |
| **OVERALL PHASE RELATIONSHIP** | | | | | | |
| $t_O$ | Phase Relation between Middle of Flyback Pulse and Middle of Sync. Pulse | | | 2.2 | | μs |
| $\frac{\Delta V_5}{\Delta t_O}$ | Adjustment Sensitivity | | | 65 | | $\frac{mV}{\mu s}$ |
| $\frac{\Delta I_5}{\Delta t_O}$ | Adjustment Sensitivity | | | 16 | | $\frac{\mu A}{\mu s}$ |

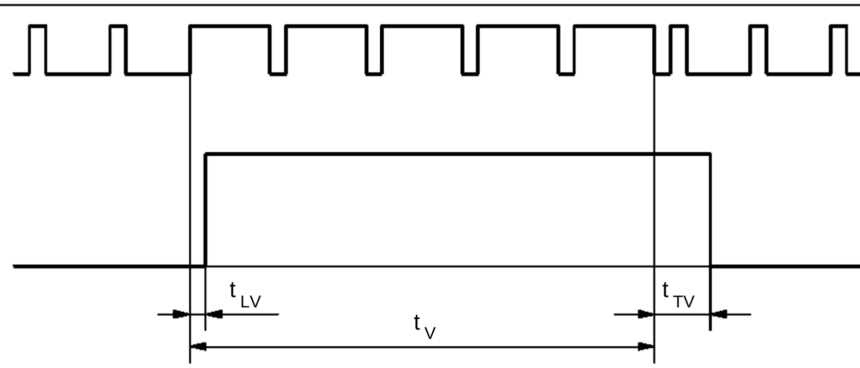
1180P-05.TBL

## TEST CIRCUIT




1180P-03.EPS

**Figure 1 :** Vertical Sync. Output Pulse




1180P-04.EPS

**Figure 2 :** Relation Ship of Main Waveform Phases

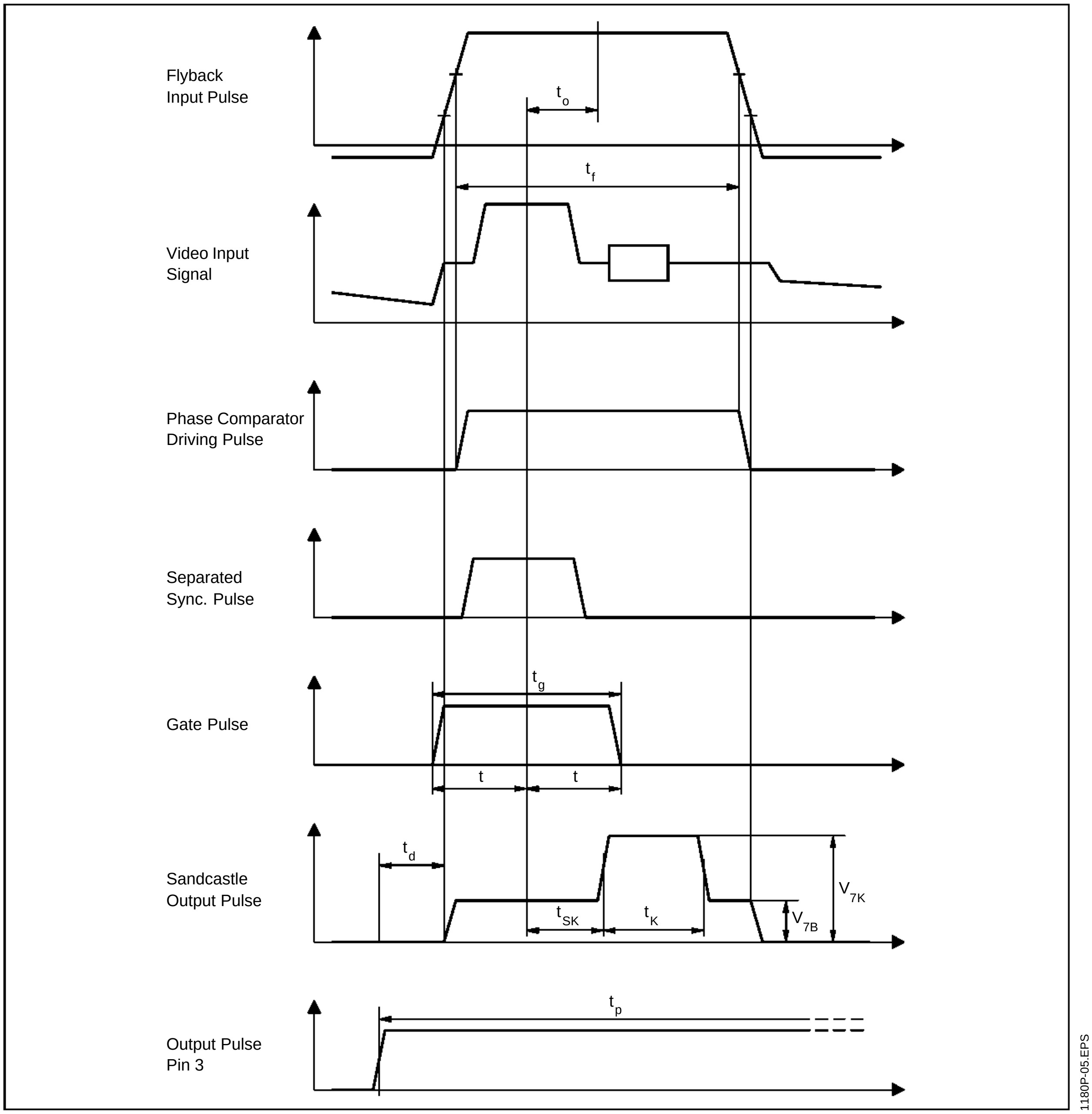


**Figure 3 :** Free Running Frequency versus Supply Voltage

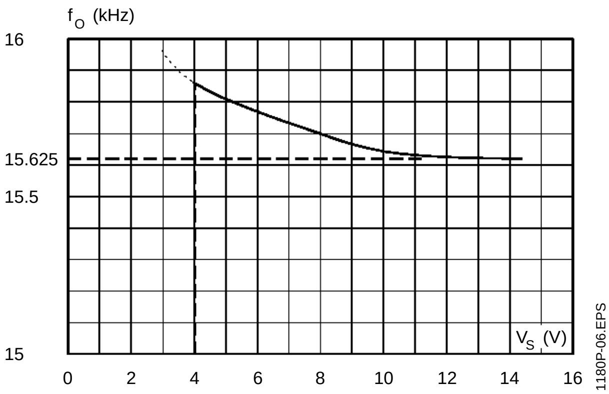
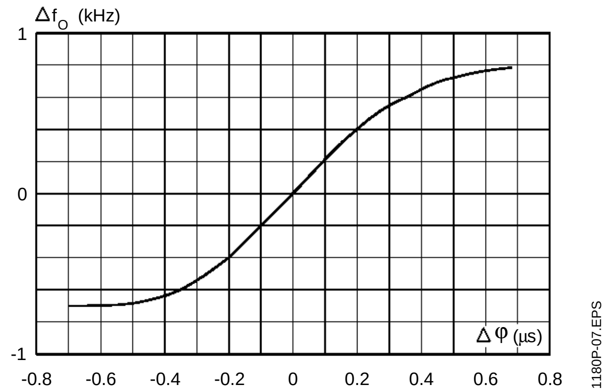



**Figure 4 :** Loop Gain




## APPLICATION INFORMATION

**Pin 1 - Positive supply**
The operating supply voltage of the device ranges from 10V to 13.2V

**Pin 2 and 3 - Output**
The outputs of TDA1180P are suitable for driving transistor output stages, they deliver positive pulse at Pin 3 and negative pulse at Pin 2.
The negative pulse is used for direct driving of the output stage, while positive pulse is useful when a driver stage is required.
The rise and fall times of the output pulses are about 150 ns so that interference due to radiation are avoided.
Furthermore the output stages are internally protected against short circuit.

**Pin 4 - Protection circuit input**
By connecting Pin 4 of the IC to earth the output pulses at Pin 2 and 3 are shut off ; this function has been introduced to produced to protect the final stages from overloads.
The same pulses are also shut off when the supply voltage falls below 4V.

**Pin 5 - Phase shifter filter**
To compensate for the delay introduced by the line final stages, the flyback pulses to Pin 6 and the oscillator waveform are compared in the oscillator-flyback pulse phase comparator.
The result of the comparison is a control current which, after it has been filtered by the external capacitor connected to Pin 5, is sent to a phase shifter which adequately regulates the phase of the output pulses.
The maximum phase shift allowed is: $t_d = t_p - t_f$ where $t_f$ is the flyback pulse duration.
Pin 5 has high input and output resistance (current generator).

**Pin 6 - Flyback input**
The flyback pulse drives the high impedance input through a resistor in order to limit the input current to suitable maximum values.
The flyback input pulses are processed by a double threshold circuit; this generates the blanking pulses by sensing low level flyback voltage and the pulses to drive the phase comparator by sensing high level flyback voltage, therefore phase jitter caused by ringing normally associated with the flyback pulse, is avoided.

**Pin 7 - Key and blanking pulse output**
The key pulse for taking out the burst from the chrominance signal is generated from the oscillator ramp and has therefore a fixed phase position with respect to the sync.
The key pulse is then added internally to the blanking pulse obtained by correctly forming the flyback pulse present at Pin 6.
The sum of the two signals (sandcastle pulse) is available on low impedance at output Pin 7.

**Pin 8 and 9 - Sync separators inputs**
The video signal is applied by means of two distinct biasing networks to pins 8 and 9 of the IC and therefore to the respective vertical and horizontal sync separators.
The latter take the sync pulses out of the video signal and make them available to the rest of the circuit for further processing.

**Pin 10 - Vertical sync output**
The vertical sync pulse, obtained by internal integration of the synchronizing signal, is available at this pin.
The output impedance is typically 10kΩ and the lowest amplitude without load is 11V.

**Pin 11 - Coincidence detector**
From the oscillator waveform a gate pulse 7 µs wide is taken whose phase position is centered on the horizontal synchronism.
The gate pulse not only controls a logic block which permits the sync to reach the oscillator-sync phase comparator only for as long as its duration, but also allows the latching and de-latching conditions of the oscillator to be established.This function is obtained by a coincidence detector which compares the phase of the gate pulses with that of the sync.
When the two signals are not accurately aligned in time it means that the oscillator is not synchronized. In this case the detector acts on the logic block to eliminate its filtering effect and on the time constant switching block to establish a high impedance on Pin 12 (small time constant of low-pass filter).
This latter block also acts on the oscillator-sync phase detector to increase its sensitivity and with it the loop gain of the synchronizing system.
In this conditions the phase lock has low noise immunity (wide equivalent noise bandwidth) and rapid pull-in time which allows fairly short synchronization times.
Once locking has taken place the coincidence detector enables the logic block, causes a low impedance on Pin 12 and reduces the sensitivity of the phase comparator.
In these conditions the phase lock has high noise immunity ( narrow equivalent noise bandwidth) due to the complete elimination of interference which occurs during the scanning period and the greater inertia with which the oscillator can change its frequency.
To optimize the behaviour of the IC if a video recorder is used, the state of the detector can be forced by connecting Pin 11 to earth or to + $V_S$. The characteristics of the phase lock thus correspond to the lack of synchronization.

**Pin 12 - Time constant switch,** (see Pin 11)

**Pin 13 - Control current output**
The oscillator is synchronized by comparing the phase of its waveform with that of the sync pulses in the oscillator-sync phase comparator and sending its output current I13 (proportional to the phase difference between the two signals) to Pin 15 of the oscillator after it has been filtered properly with an external low-pass circuit.
The time constant of the filter can be switched between two values according to the impedance presented by Pin 12.
The voltage limiter at the output of the phase comparator limits the voltage excursion on Pin 13 and therefore the frequency range in which the oscillator remains held-in.
The output resistance of Pin 13 is:
- low when V13 > 4.3 or V13 < 1.6V
- high when 1.6V < V13 < 4.3V

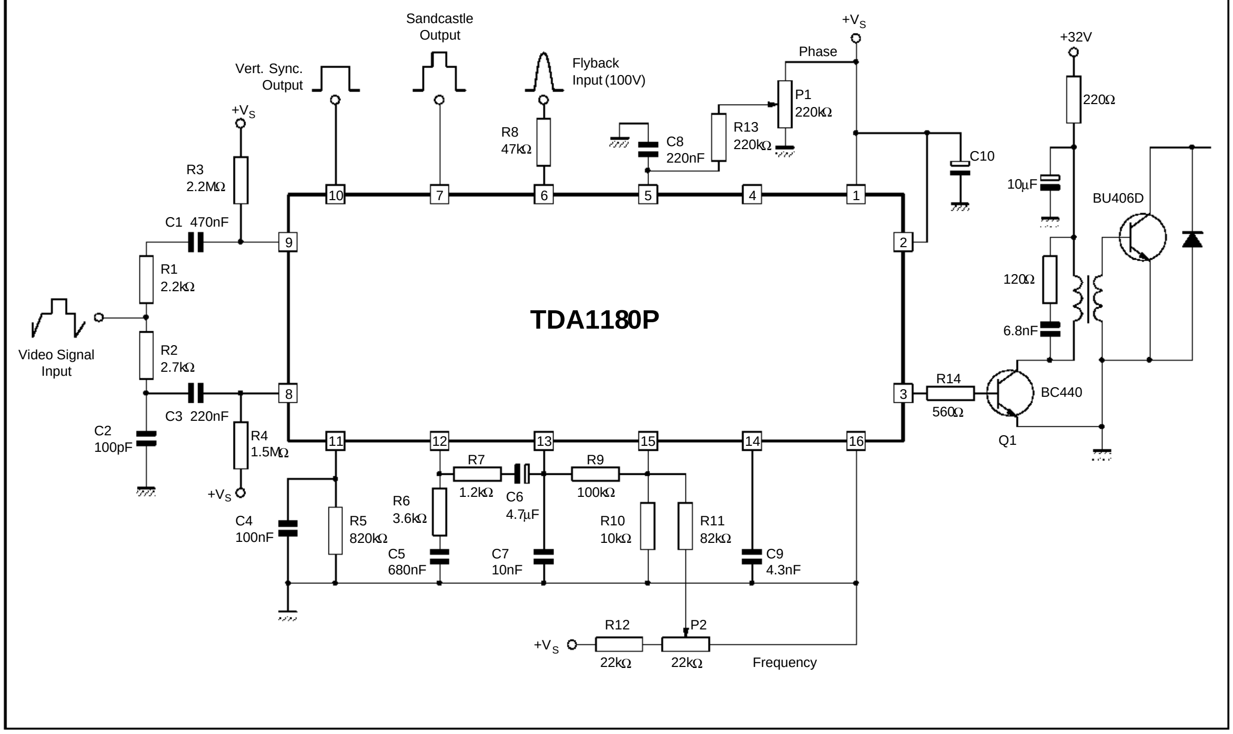
To prevent the vertical sync from reaching the oscillator-sync phase comparator along with the horizontal sync,a signal which inhibits the phase detector during the vertical interval is taken from the vertical output stage; inhibition remain even if the video signal is not present.
The free running frequenc of the oscillator is determined by the values of the capacitor and of the resistor connected to Pins 14 and 15 respectively.
To generate the line frequency output pulses, two theresholds are fixed along the fall ramp of the triangular waveform of the oscillator.

**Pin14 - Oscillator** (see Pin 13)

**Pin 15 - Oscillator control current input** (see Pin 13)

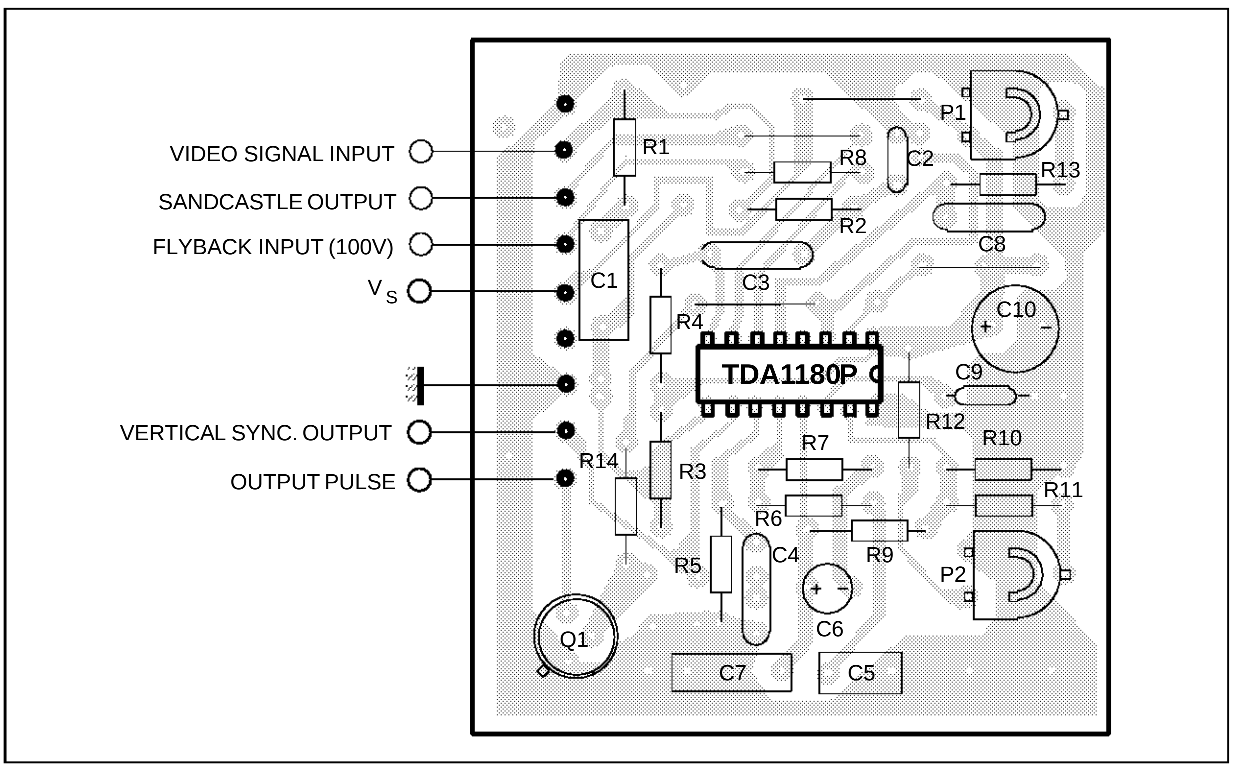
**Pin 16 - Ground**

**Figure 5 :** Application Circuit for Large Screen Black & White and Colour TV



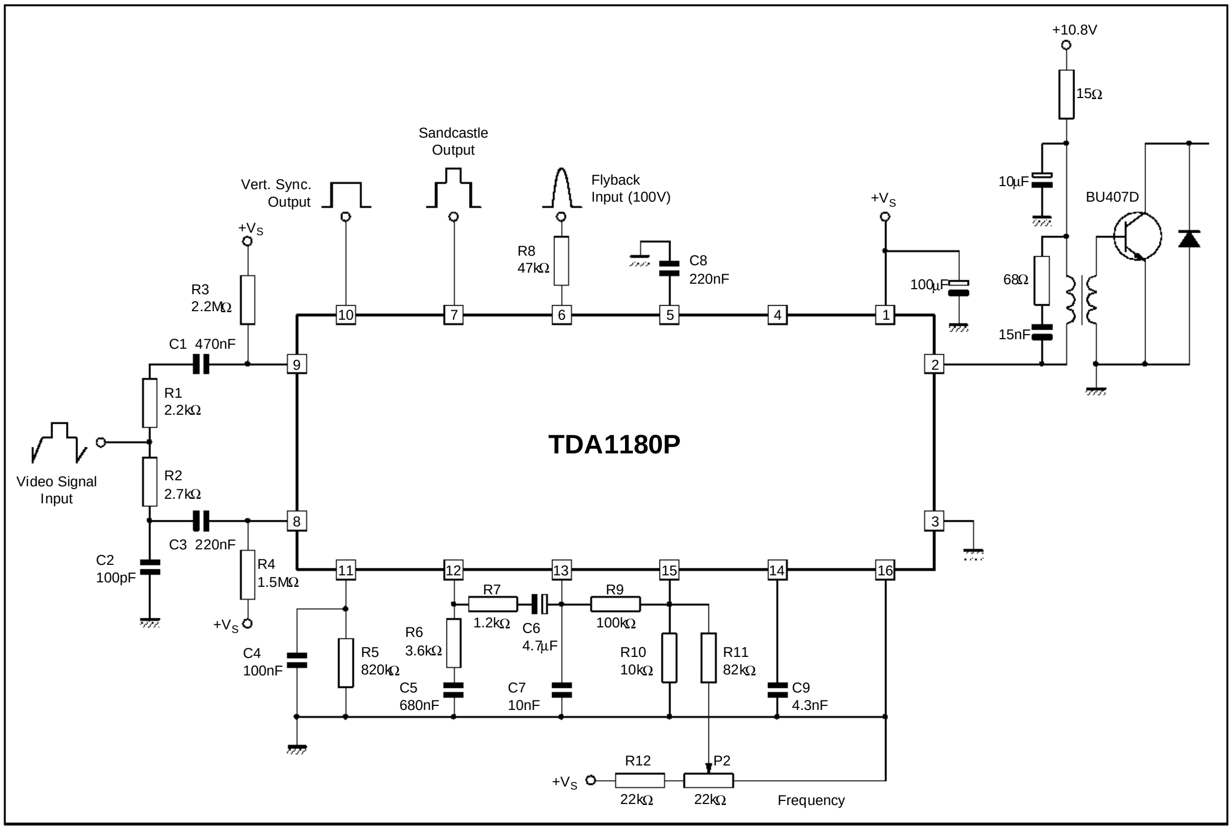

1180P-08.EPS

**Figure 6 :** P.C. Board and Component Layout for the Circuit in Figure 6 (1:1 scale)



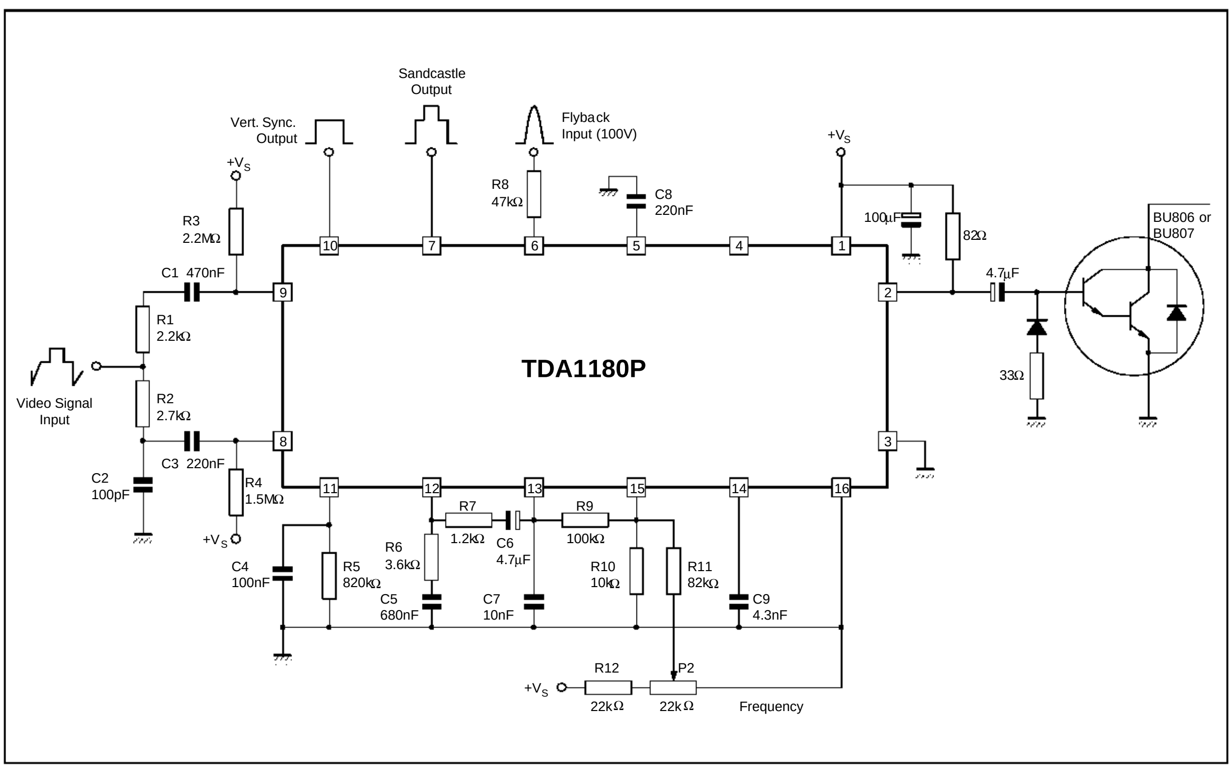

1180P-09.EPS

**Figure 7 :** Application Circuit for Small Screen b.w. TV




1180P-10.EPS

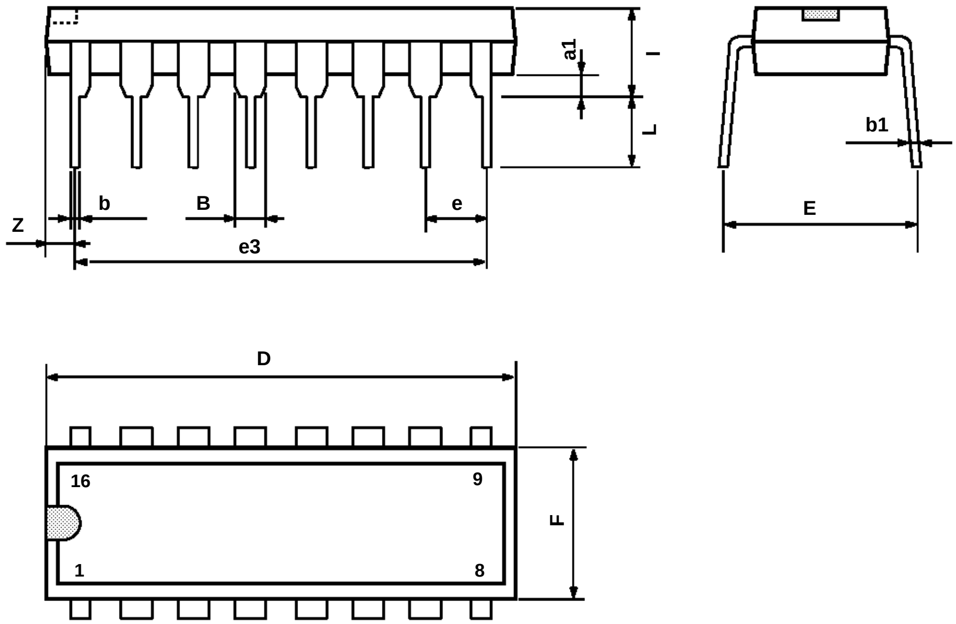
**Figure 8 :** Application Circuit for Darlington Output Stage




1180P-11.EPS

## PACKAGE MECHANICAL DATA

16 PINS - PLASTIC DIP




PM-DIP16.EPS

| Dimensions | Millimeters | | | Inches | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| a1 | 0.51 | | | 0.020 | | |
| B | 0.77 | | 1.65 | 0.030 | | 0.065 |
| b | | 0.5 | | | 0.020 | |
| b1 | | 0.25 | | | 0.010 | |
| D | | | 20 | | | 0.787 |
| E | | 8.5 | | | 0.335 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 17.78 | | | 0.700 | |
| F | | | 7.1 | | | 0.280 |
| i | | | 5.1 | | | 0.201 |
| L | | 3.3 | | | 0.130 | |
| Z | | | 1.27 | | | 0.050 |

DIP16.TBL